Bi-weekly Status Report 3
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:
Over the course of the last two weeks, we did the following: implemented the serial communication from the CyDaq to Matlab; investigated the use of FreeRTOS in the FPGA; continued work on the 324 and heart rate labs; designed input gain stage and protection; and physically assembled data conversion evaluation module. We also brainstormed different ways to implement a mass damper lab that is both simple to construct and accurate all at a low cost for the electrical department.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 13; Cumulative: 110)**
  - Completed first RTOS firmware architecture
    - Developed UART communication task
    - Developed XADC sampling task
  - Prototyped interrupt-based firmware architecture to improve sampling rate
  - Began researching XADC DMA strategies to improve sampling rate
- **Sam Burnett (Bi-weekly: 20, Cumulative: 121)**
  - Physically assembled data conversion evaluation module
  - Designed multiple feedback anti-aliasing filter
  - Simulated anti-aliasing filter design in SPICE
  - Designed input gain stage and protection
- **Mitchell Hoppe (Weekly: 12; Cumulative: 98.0)**
  - Added quality of life improvements to the front end of the user interface.
  - Fixed bugs related to pythons interactions over serial.
  - Enabled the user to Start and Stop sampling the DAQ and save the fetched samples to a file.
- **Max Kiley (Biweekly: 10; Cumulative: 111)**
  - Began reviewing EE 324 learning objectives to accompany the lab
  - Building and measuring step response for RLC circuit for lab 1
  - Simulating step response using Matlab
  - Brainstorming ideas for spring mass damper mechanical system.
- **Emily LaGrant (Biweekly: 12; Cumulative: 103)**
  - Attended weekly meetings to plan project demo
  - Worked on draft for image restoration lab
  - Made minor changes to heart rate lab
- **Isaac Rex (Bi-Weekly: 12.5; Cumulative: 166)**

    - Tackled issues found when designing controls 1 lab
    - Finished Labview script for use with Keysight DSO
    - Worked on concept ideas for FIR and difference equation labs

Pending Issues:

- Fabrication of data acquisition evaluation board was challenging (small packages)
- Signal path and SPI communication functionality needs to be tested off system
- FreeRTOS tick rate is limited to 1kHz, which anvasmeans tasks can't run for less than 1 ms, a major problem when the XADC sampling task needs to run at upwards of 2 MHz.

Plans:

- Isaac:
    - Adapt Labview script to work with DAD
    - Continue writing lab documents
    - Finish controls 1 lab by Sunday Oct. 4th
    - Start controls 2 lab
- Emily:
    - Continue working on image restoration lab
    - Test image restoration lab
    - Work on faculty demo of CyDAQ
- Brady:
    - Demonstrate CyDAQ to our client, Matt Post
    - Clean up RTOS firmware structure and finish interrupt-based simple architecture
    - Investigate possible solutions to FreeRTOS tick rate issue, including alternatives to FreeRTOS
- Sam:
    - Validate / Test analog signal path of fabricated evaluation board
    - Validate / Test SPI communication functionality for evaluation board
    - Start master board layout modifications for the added ADC and DAC
    - Integrate MF glitch filter into ADC front end layout.
- Max
    - Continue simulating RLC step response.
    - Begin creating a draft of lab 1 for EE 342
    - Start creating a prototype of the mass-spring-damper-system
- Mitch
    - Change the sampling mode on the Front end and the CyDaq to streaming mode, so we can fetch the samples as they arrive. Instead of all at once at the end of the sampling period.
    - Have the Matlab front end automatically add the python scripts to the User PATH of windows if it is not already there.